

Introduction to comparators, their parameters and basic applications

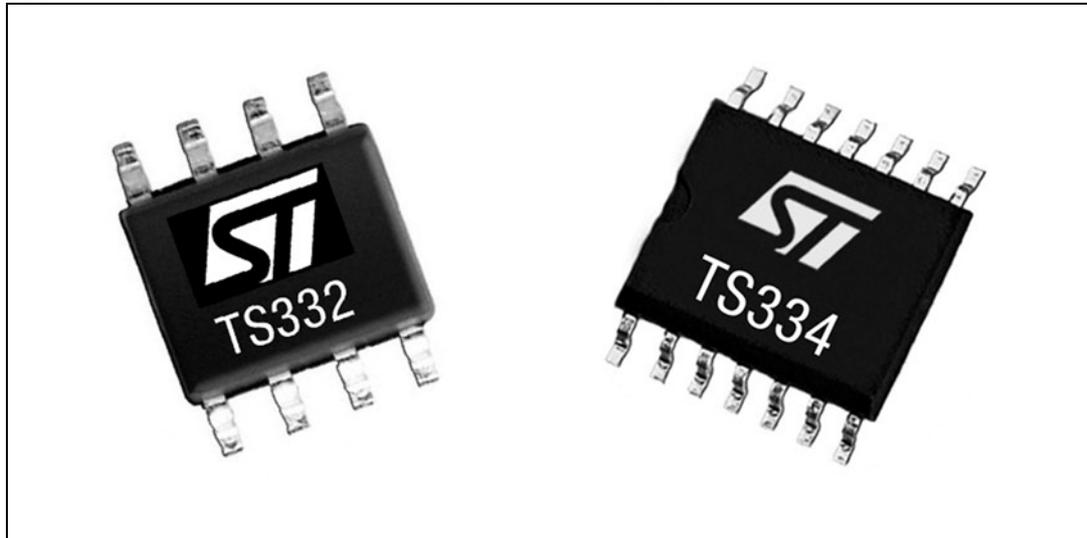
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Introduction

After operational amplifiers (op amps), comparators are the most generally used analog, simple integrated circuits.

Operational amplifiers are well described in many publications and a lot of information can be found regarding the design and proper use of these devices. On the other hand, information concerning comparators is much harder to find as they are often considered as simple devices. This note explains the main parameters of comparators and their limitations from an application point of view.

Figure 1. TS332 and TS334 micropower low-voltage rail-to-rail comparators



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1 Comparator substitution by an op amp

To use operational amplifiers in open loop as comparators is quite common. This especially applies when an op amp is already used in the application, giving the user the opportunity to use a dual channel (or quad channel) op amp which can save space in the application. This is possible even if a better alternative is to use comparators that are optimized for this purpose.

The op amp is a device which is designed to be used with negative feedback. A major concern is to ensure the stability of such a configuration. Other parameters like slew rate and maximum bandwidth are trade-offs with current consumption and the architecture of an op amp.

Comparators, on the other hand, are designed to operate in open loop configuration without any negative feedback. In most cases, they are not internally compensated. The speed (propagation delay) and slew rate (rise and fall time) are maximized. The overall gain is also usually higher. The use of an op amp as a comparator leads to an unoptimized situation, where current consumption versus speed ratio is low. The opposite is even worse. Normally, a comparator cannot be used instead of an op amp. Most probably, the comparator shows instability under negative feedback. Generally speaking, comparators and operational amplifiers cannot substitute each other except for low performance designs.

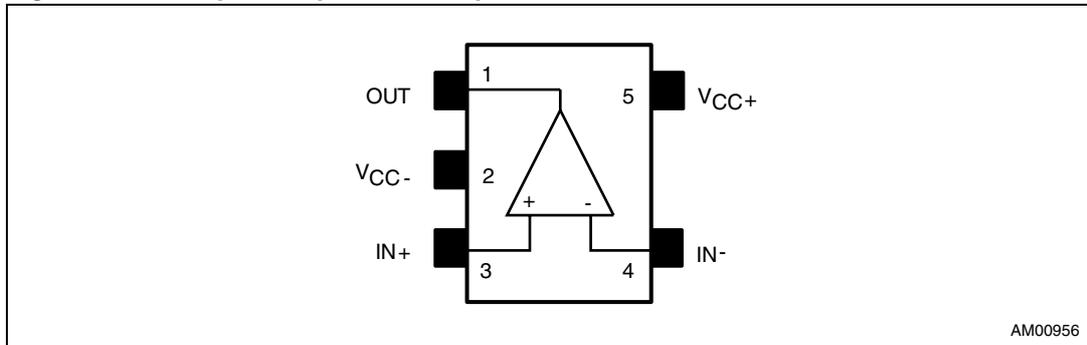
2 Comparator parameters

Comparator classification by major parameters

- Propagation delay
- Current consumption
- Output stage type (open collector/drain or push-pull)
- Input offset voltage, hysteresis
- Output current capability
- Rise and fall time
- Input common mode voltage range.

Besides major parameters, comparators are classified by other parameters such as input bias current, common mode and power supply rejection ratio, sample/hold function, and startup time.

Figure 2. Comparator pinout example

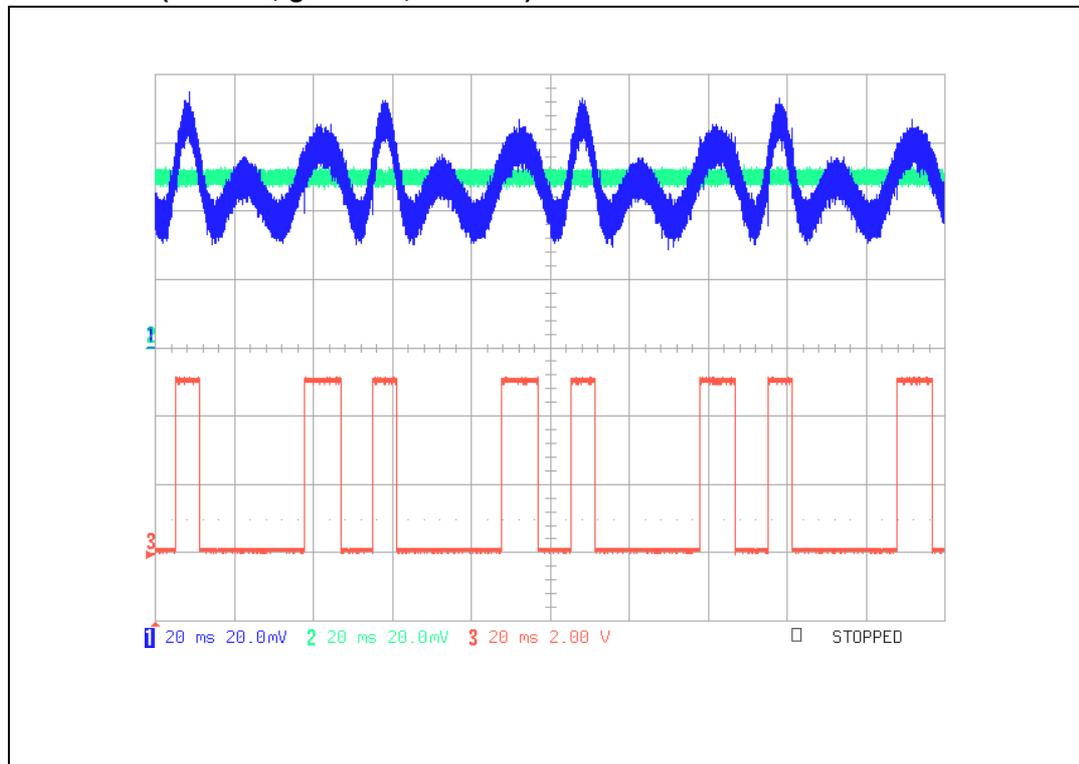


A single device has, ordinarily, five pins: two for power supply V_{CC+} , V_{CC-} , two as inputs $IN+$, $IN-$ and one for the output OUT . It is possible to have an extra pin for standby function.

When $V_{IN(+)} > V_{IN(-)}$, the output is in high state, if $V_{IN(+)} < V_{IN(-)}$, the output is in low state.

Figure 3 shows the comparison made by a TS3011 comparator between a 20 m V_{PP} input signal (blue) applied on IN+ and a 50 mV DC reference voltage (green) applied at IN-. The output signal (red) amplitude is 5 V. As can be seen, sometimes, the input signal exceeds the reference voltage though the output remains low. This is caused by the internal hysteresis voltage of the TS3011. Hysteresis is discussed in Section 4.

Figure 3. Signal comparison by TS3011 with built-in hysteresis (blue IN+, green IN-, red OUT)



Concerning the output configuration, there are two main types of comparators: with push-pull and open collector (or open drain). Push-pull stage output levels are typically V_{CC} and 0 V (voltage drop from power supply pins can be neglected). In the case of open collector configuration, an external pull-up resistor is used. Such a configuration allows an external voltage to be applied, different from V_{CC}, to drive the high level state. Pull-up configuration can be used as a simple voltage level translator. The second advantage of a device with open collector is that more outputs can be connected together. This is useful for wired-OR configuration systems. It is also possible to find comparators with a differential output stage. These devices are less common and mainly used in telecommunication systems as transmission line drivers. For example, the TS3021, TS3011 and TS861 are STMicroelectronics® comparators with push-pull output stage while the LMV331, TS7221 and TS331 are open drain configuration.

Figure 4. Open drain

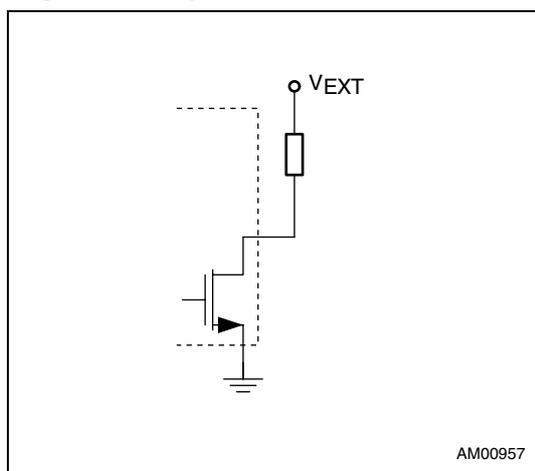


Figure 5. Push-pull

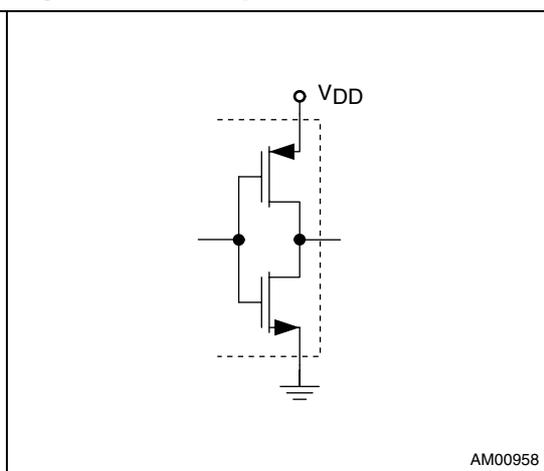
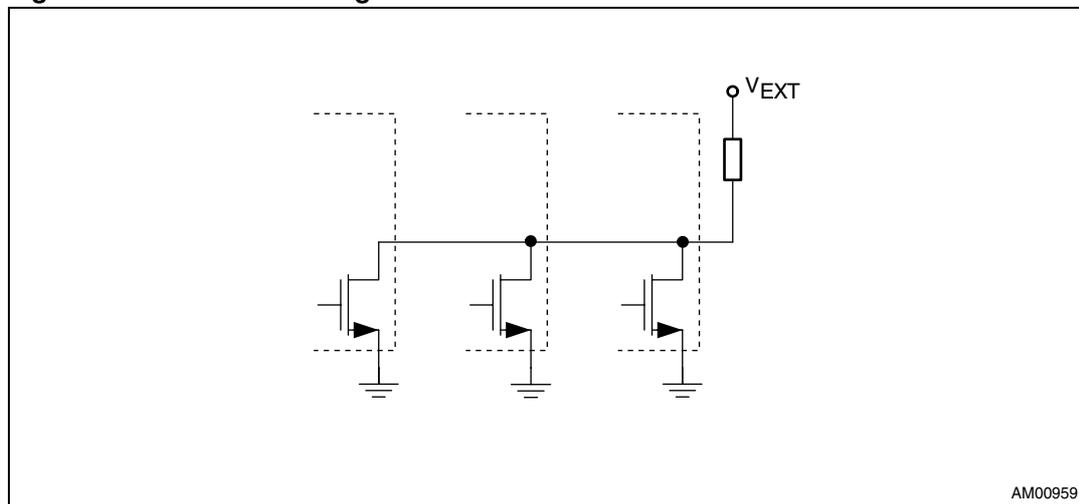


Figure 6. Wired-OR configuration



3 Datasheet parameters

3.1 Input common mode voltage range - V_{ICM}

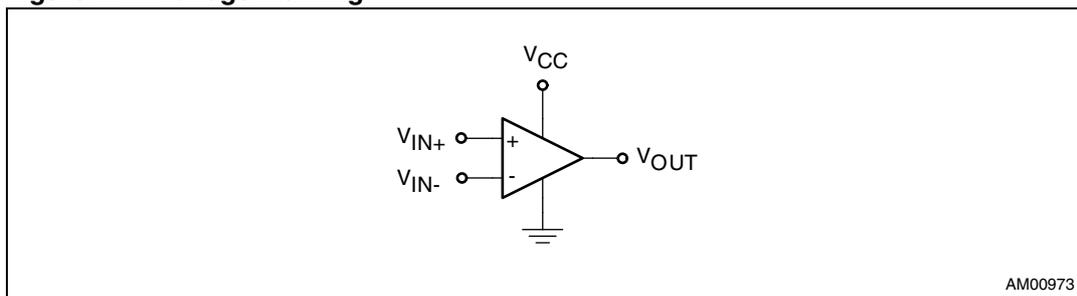
The V_{ICM} is defined as the voltage range where both inputs must remain to guarantee the functionality of the device. When the input common mode range covers both power supply rails 0 V and V_{CC} , it is a rail-to-rail input stage.

Regarding the use of a rail-to-rail (R2R) comparator, from a technical point of view, if the R2R input capability is not needed, it is always better to choose a comparator without R2R input stage. The power consumption is, in that case, obviously smaller and the device cost is lower.

3.2 Input offset voltage - V_{IO} (V_{TRIP})

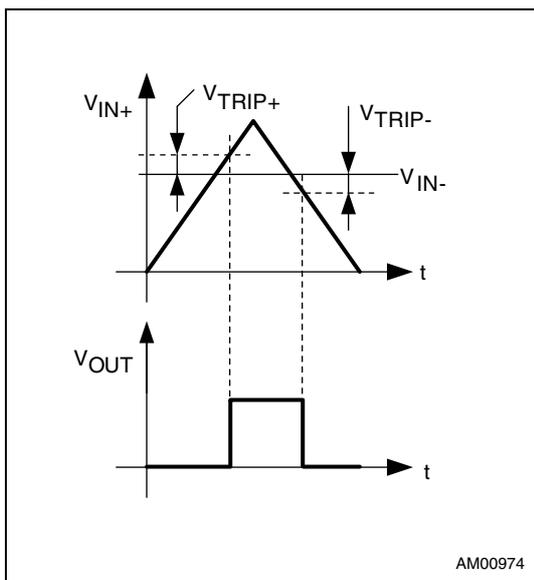
The input offset voltage (V_{IO}) can be defined as the differential input voltage to apply in order to be at the toggling level. Input offset voltage limits the resolution of comparators. Therefore, for very small signals (in the same order as the V_{IO}), the comparator toggles at an undesired value or does not toggle at all.

Figure 7. Voltage marking



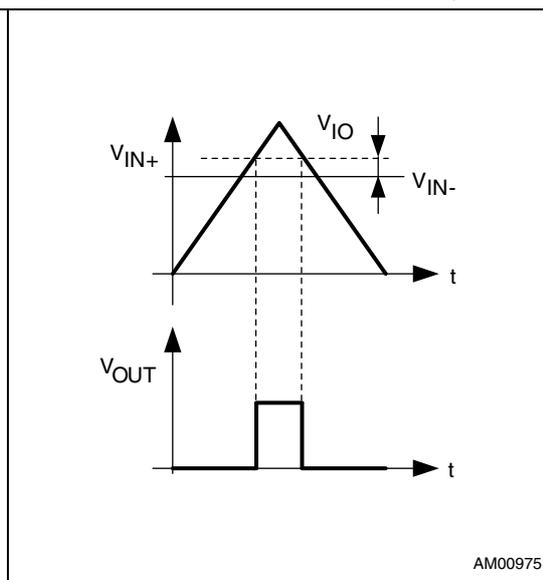
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Figure 8. Input-trip point V_{TRIP}



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Figure 9. Input offset voltage V_{IO}



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In other words, input offset voltage can be represented by a voltage source applied in series with one input of an ideal comparator. Consequently, the output doesn't toggle when $V_{IN+} = V_{IN-}$, as in the case of an ideal comparator, but the threshold level is shifted by the input offset value V_{IO} . Input offset voltage rises in the input stage as a consequence of transistor imbalance. For comparators with built-in hysteresis, V_{IO} is defined as the average value of V_{TRIP+} and V_{TRIP-} , and the hysteresis of $V_{HYST} = V_{TRIP+} - V_{TRIP-}$, where V_{TRIP+} (respectively V_{TRIP-}) is the input differential voltage for which the output switches from low to high state (respectively high to low state).

Measurement

Input offset voltage and trip points can be measured using the circuit shown in [Figure 10](#). The first DC source sets the power supply V_{CC} and the second sets V_{ICM} , the common mode voltage. A 100 mV_{PP} triangle signal is applied on the voltage divider (1/101). The voltage divider is necessary to obtain a good accuracy on the V_{IO} reading by the scope, and to use the function generator with an amplitude that it can handle. The triangle signal should be low frequency (20 Hz); higher frequency can lead to error in the V_{IO} measurement caused by propagation delay of the device. When the output changes its state, the actual input voltage value V_{IN} is read from the scope, from V_{IN} we can simply deduce $V_{IO} = V_{IN} / 101$.

Pay attention to the fact that the oscilloscope probes and waveform generator ground are on the inverting input pin of the comparator. Therefore, V_{ICM} and V_{CC} power supplies must be floating from earth-ground, or an isolation transformer must be used. The advantage is that the V_{ICM} voltage does not need to be subtracted from the V_{IO} reading. V_{ICM} can be easily changed without having to adjust the offset of the input signal, making the measurement more comfortable.

Figure 10. V_{IO} (V_{TRIP}) measurement circuit

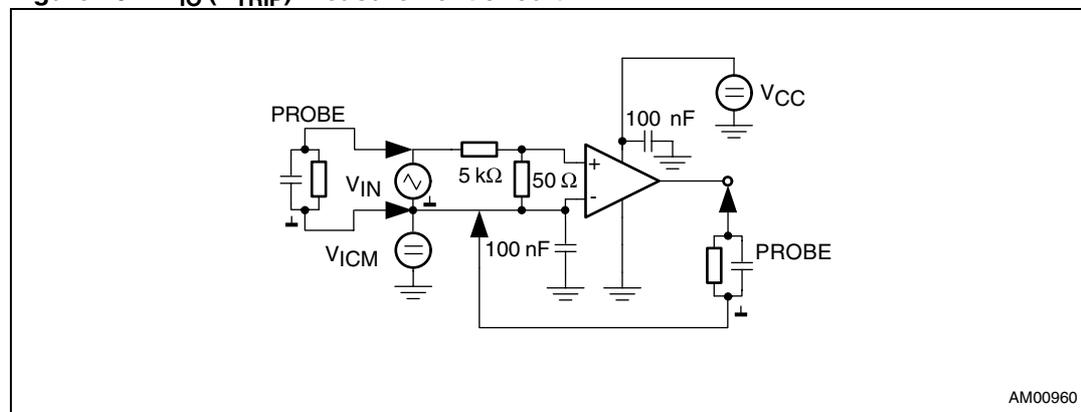
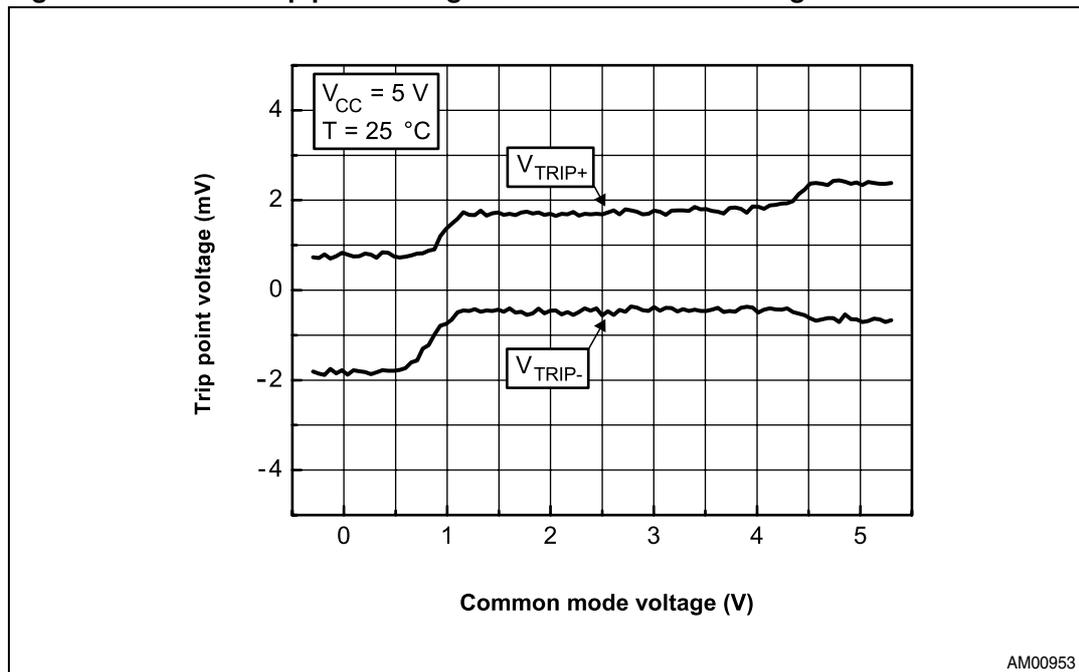


Figure 11. TS3011 trip point voltage vs. common mode voltage



Use passive oscilloscope probes with 10:1 dividing ratio. For increased accuracy on V_{IO} reading and decreased noise background, the probe applied at V_{IN} can be replaced by a coaxial cable. Unlike propagation delay (T_{PD}) measurement, the cable capacity doesn't have an impact here because the frequency of V_{IN} is low.

Figure 11 is an example of the measured V_{IO} vs. V_{ICM} for the TS3011 which is a high speed rail-to-rail comparator from STMicroelectronics. The effect of the two input stages can be clearly seen. Each stage has a different V_{IO} with its own dependency on V_{ICM} . One stage is operating up to $V_{ICM} = V_{CC} - 0.7 V$ while the second one covers the range from 0.7 V to V_{CC} . The overall curve is the merging of both stages. It can be understood from the presence of two V_{TRIP} curves that the TS3011 has a built-in hysteresis.

3.3 CMRR and SVR

The “common mode voltage rejection ratio” (CMRR) describes the relationship between input offset voltage V_{IO} and the input common voltage V_{ICM} . It is defined as V_{ICM} over V_{IO} variation ratio, and is usually represented in logarithmic scale.

Equation 1

$$CMRR [dB] = 20 \cdot \log (| \Delta V_{ICM} / \Delta V_{IO} |)$$

CMRR is calculated with two values of input offset voltages measured for two different input common mode voltages (usually 0 V and V_{CC}).

The “supply voltage rejection” (SVR) is a parameter describing the relation between the input offset voltage V_{IO} and the power supply voltage. The power supply voltage modification may affect, more or less, the bias of the input differential transistor pairs. It means that the input offset voltage is also slightly modified.

Equation 2

$$\text{SVR [dB]} = 20 \cdot \log (|\Delta V_{CC} / \Delta V_{IO}|)$$

Note that, the higher CMMR and SVR are the better.

Measurement

The circuit is the same as the one used for V_{IO} ([Figure 10](#)).

1. CMRR
 V_{IO} at low (L) V_{ICM} rail and V_{IO} at high (H) V_{ICM} rail are measured
then $\text{CMRR} = 20 \cdot \log [(V_{ICM(H)} - V_{ICM(L)}) / (|V_{IO(H)} - V_{IO(L)}|)]$
2. SVR
 V_{IO} at low V_{CC} and V_{IO} at high V_{CC} are measured
then $\text{SVR} = 20 \cdot \log [(V_{CC(H)} - V_{CC(L)}) / (|V_{IO(H)} - V_{IO(L)}|)]$

3.4 Voltage gain

Voltage gain A_{VD} indicates the overall device gain. Higher gain means better small input signal resolving capability which can be an advantage in certain applications. Common comparators have an A_{VD} in the range of 200 V/mV (106 dB). 1 mV input signal amplified by 106 dB leads to theoretical amplitude of 200 V. In reality, the output signal swing is limited by V_{CC} . Note that the A_{VD} doesn't affect external hysteresis as the output is always in high or low state and never between (unlike an operational amplifier, a comparator is not used in its linear region).

3.5 Propagation delay

Propagation delay T_{PD} is one of the key parameters for many applications because it limits the maximal input frequency which can be processed. Voltage comparison of analog signals requires a minimum amount of time.

T_{PD} is defined as the time difference between the moment the input signal crossing the reference voltage and the moment the output state changes (usually when the output signal crosses 50% of V_{CC} , if nothing is specified).

A graphical interpretation is shown in [Figure 12](#) and [13](#). For T_{PLH} an input square signal from -100 mV to $+V_{OV}$, called overdrive voltage and referenced to $V_{ICM} + V_{TRIP+}$, is applied on the non-inverting input. The inverting input is connected at V_{ICM} voltage. Initial signal condition 100 mV below $V_{ICM} + V_{TRIP+}$ ensures a sufficient saturation for the input stage. For the falling edge propagation delay measurement (T_{PHL}), the input signal goes from +100 mV to $-V_{OV}$ referenced to $V_{ICM} + V_{TRIP+}$.

Figure 12. T_{PLH} diagram

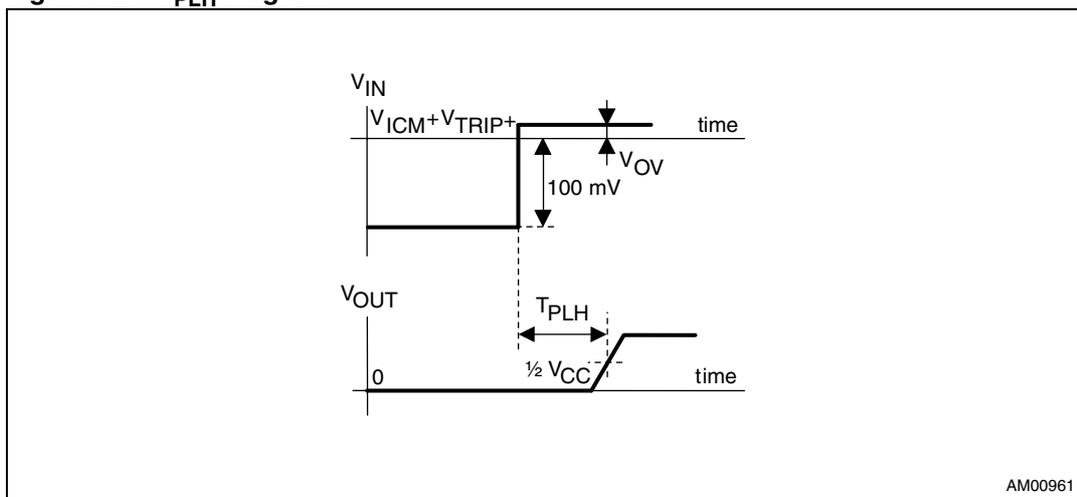
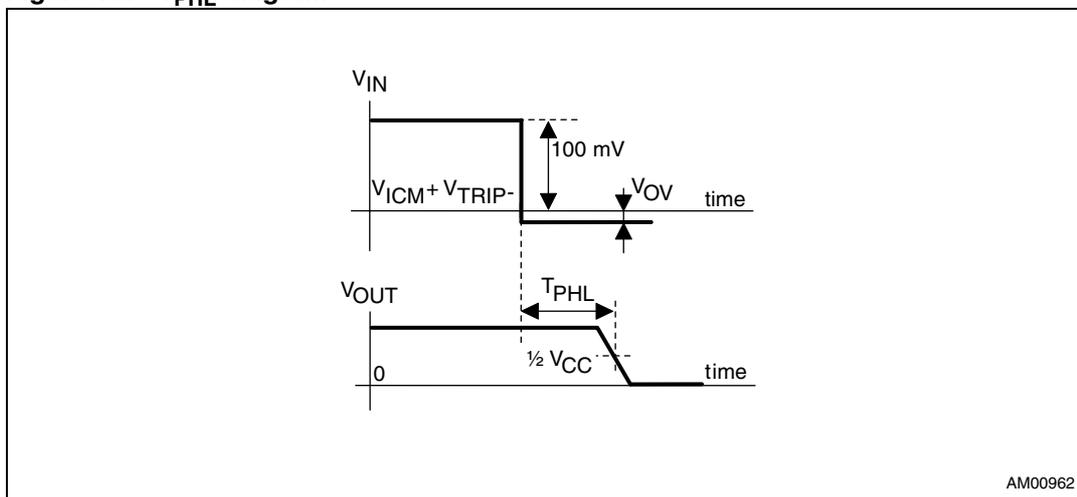


Figure 13. T_{PHL} diagram



The input signal is referenced to $V_{ICM} + V_{TRIP}$ and not only to V_{ICM} because, in the case of small signal overdrive, an error in T_{PD} measurement can occur due to non-zero V_{IO} (V_{TRIP+} and/or $V_{TRIP-} \neq 0$). In reality, we can neglect V_{IO} without significant impact on T_{PD} for V_{OV} values of 20 mV and higher, considering that the offset value reaches around 1 mV and considering the exponential dependency of T_{PD} on overdrive voltage, as shown in [Figure 14](#).

Figure 14. TS3011 T_{PD} vs. overdrive voltage

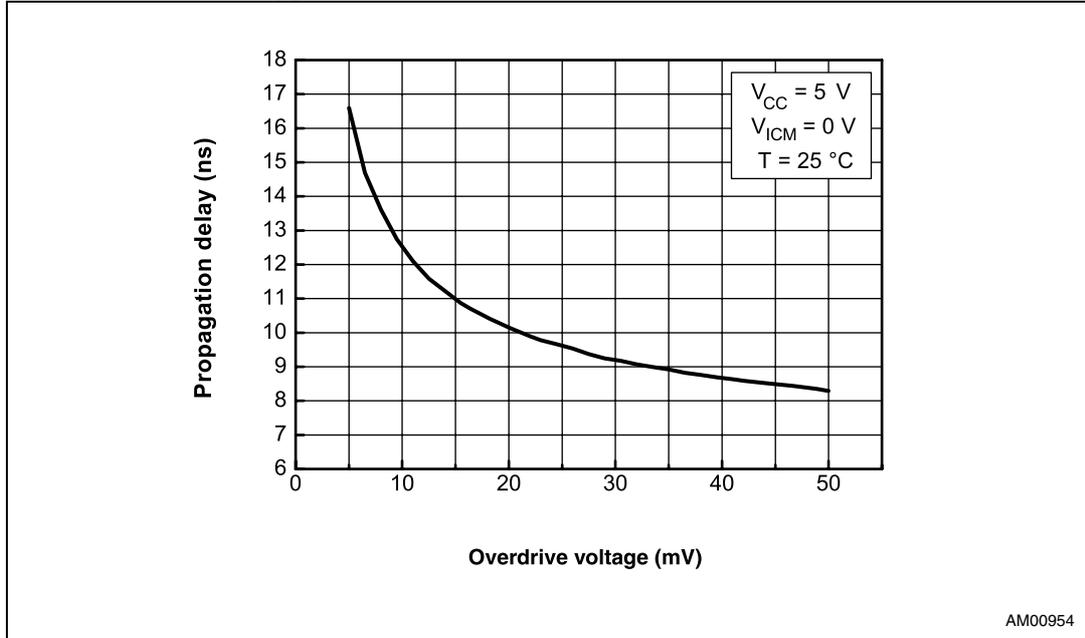
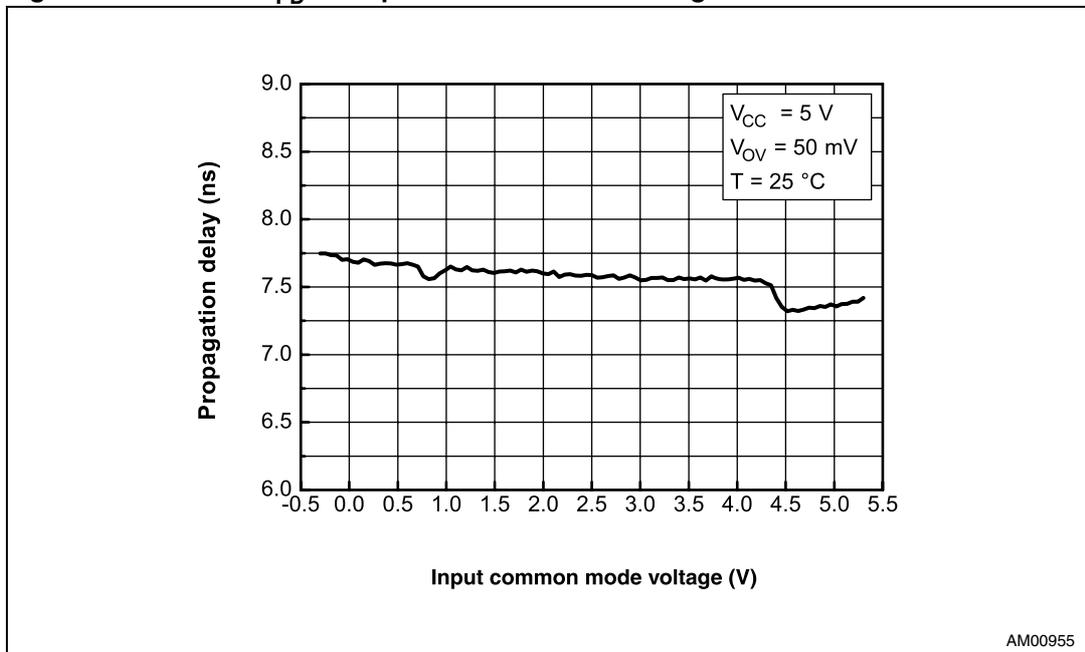


Figure 15. TS3011 T_{PD} vs. input common mode voltage

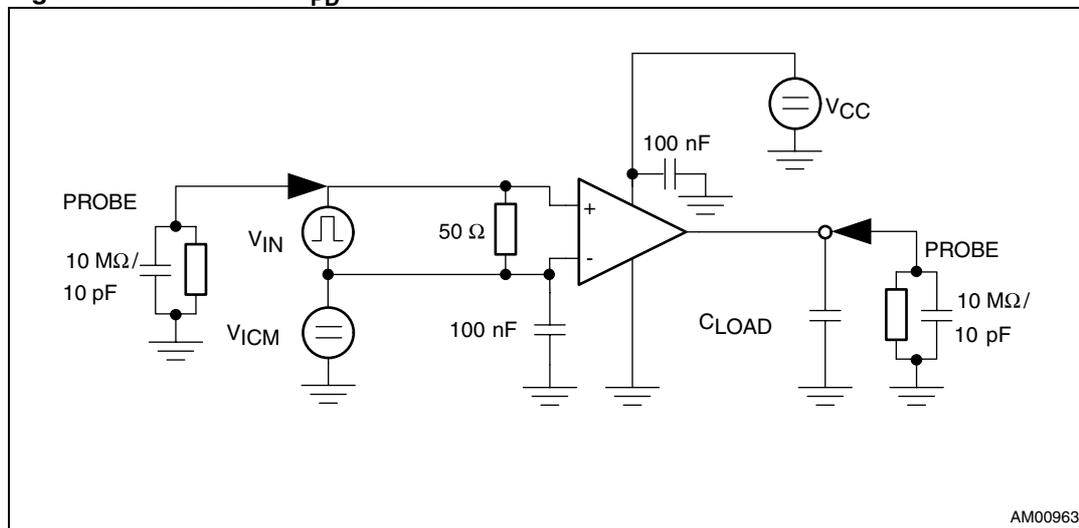


Measurement

A basic circuit for T_{PD} measurement is shown in *Figure 16*. One DC power supply is used for V_{CC} biasing, and a second one for V_{ICM} voltage. If the measurement is performed at $V_{ICM} = 0$ V, the source can be removed and the inverting pin directly connected to ground. To keep low source impedance and prevent from parasitic oscillation during switching, a 100 nF bypass capacitor is connected close to the positive supply pin V_{CC+} of the comparator. A second bypass capacitor should be connected to the comparator input pin I_{IN-} when V_{ICM} source is used. A 50 Ω resistor minimizes the effect of input pin capacitance and avoids signal reflection on the line matching the impedance at inputs of the comparator with the impedance of generator (V_{IN}).

It is necessary to define exactly the measurement conditions, especially the load capacitance C_{LOAD} which has a big impact on output signal edge speed, consequently, also on the T_{PD} value (measured at 50% of V_{OUT}). The C_{LOAD} represents the overall capacitive loading at the comparator output including loading capacitor, oscilloscope probe capacity and parasitic capacity of the PCB track.

Figure 16. Circuit for T_{PD} measurement



Many pulse generators, despite great performance in the time-base, are not able to provide accurate signal amplitude, especially for low output voltage. Generating 5 mV overdrive may be a problem because such a value is often below the generator accuracy. Therefore, for small overdrive measurement, it is more suitable to place a 50 Ω attenuator (divider bridge), instead of a single 50 Ω resistor, and increase the generator amplitude. In this way, a good amplitude accuracy can be obtained with low overdrive values.

High speed signal processing

For high-speed signal applications, more attention (at PCB level) must be paid to: proper low resistive grounding, short tracks and quality SMD capacitors having low ESR. Bypass capacitor stores charge and provides supplementary source when spikes occur on the V_{CC} line. Each real capacitor has resonant frequency where its impedance reaches the lowest value. If the input signal frequency is far from the resonant frequency, impedance strongly increases and the capacitor loses bypassing capability. Placing different capacitors with different resonant frequencies therefore allows a wide frequency bandwidth to be covered.

Such a bypass combination, made from 100 nF, 10 nF and 1 nF in parallel, eliminates unwanted spikes on the V_{CC} line much better than only one 100 nF capacitor.

Each mm of the track plays a role. Bypass capacitors must be placed as close as possible to the comparator supply pin. Place the smallest capacitor closer to the supply pin than the bigger one. Removing GND copper under signal track minimizes overall capacitive loading. Input source impedance shouldn't exceed 1 k Ω otherwise undesirable oscillations can appear. In addition, too high input impedance in series with parasitic PCB capacity and input comparator capacity produces additional RC constant which means additional propagation delay.

Concerning time measurements on high-speed comparators, remember that for a high speed signal the oscilloscope and probe can cause significant error in measurement accuracy when their bandwidth is too low. The measured T_{RISE} (T_{FALL}) value is affected by the rise time of the scope and the probe by:

Equation 3

$$T_{RISE} = (T_{RISE\ SIGNAL}^2 + T_{RISE\ SCOPE}^2 + T_{RISE\ PROBE}^2)^{1/2}$$

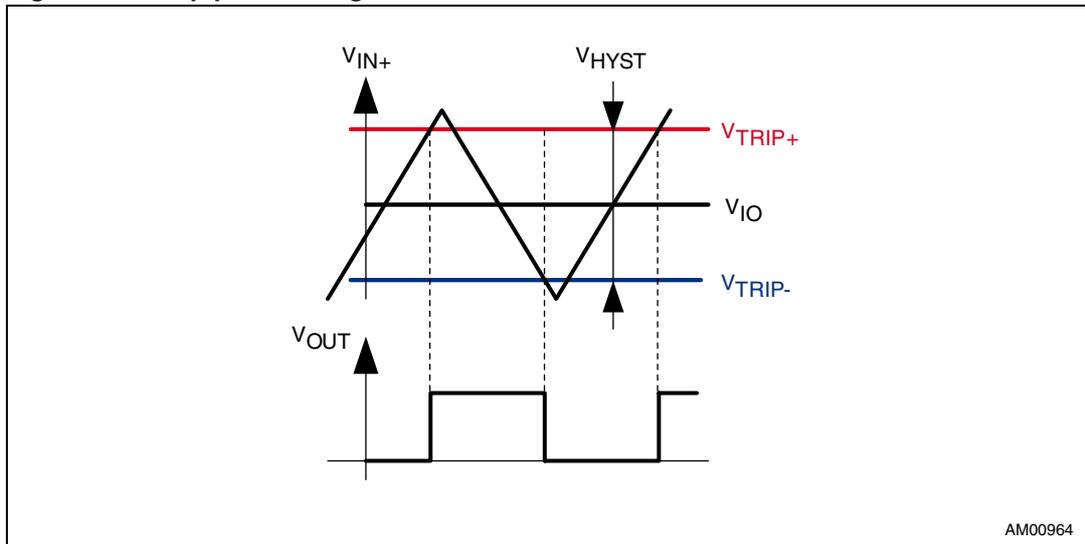
4 Hysteresis

For slow time changing input signal, an output oscillation can appear while the input signal remains close to the reference voltage. Also low amplitude signal on high impedance can cause oscillations due to noise background. Such unwelcome behavior can be solved by hysteresis. The principle of hysteresis consists of two different input threshold voltages depending on actual output state.

4.1 Built-in hysteresis

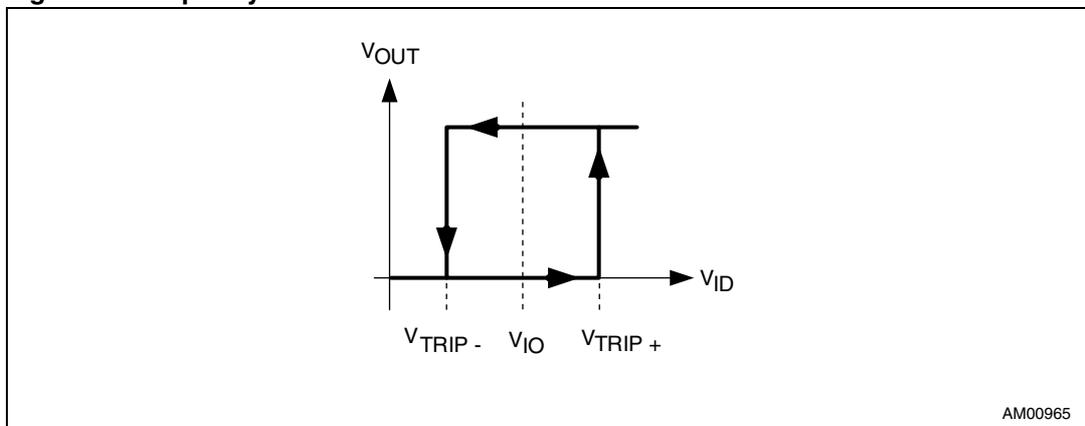
Many comparators have built-in hysteresis. Typical hysteresis value is a few mV. This is enough to suppress output undesired toggling in most cases but it doesn't impact significantly the resolution of the comparator. For comparators with built-in hysteresis, the average lower and upper threshold voltage is computed and referred as input offset voltage V_{IO} , the V_{TRIP+} and V_{TRIP-} difference is referred as hysteresis voltage V_{HYST} and is shown in [Figure 17](#).

Figure 17. Trip point voltage definition



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Figure 18. Input hysteresis

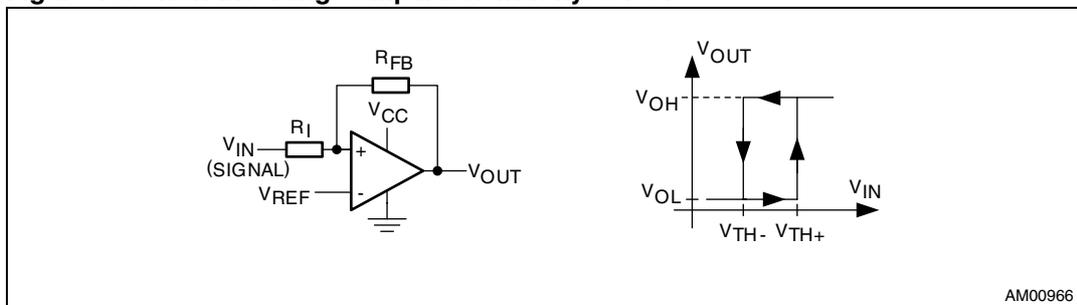


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4.2 External hysteresis

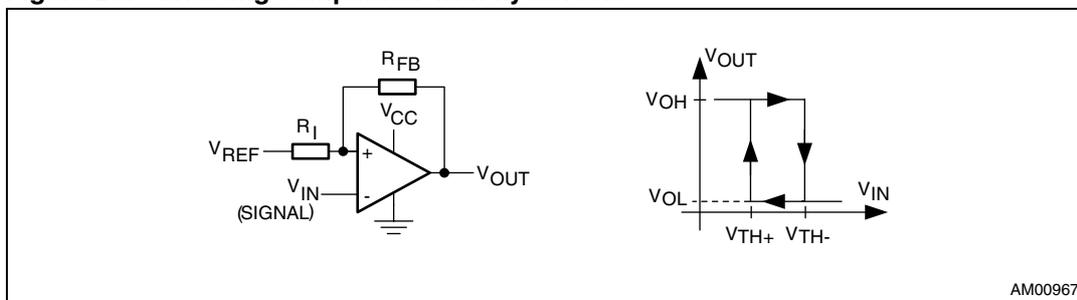
If the device doesn't include built-in hysteresis, or if a large hysteresis is required, a positive feedback network can be implemented. [Figure 19](#) shows a non-inverting and [Figure 20](#) an inverting comparator with hysteresis.

Figure 19. Non-inverting comparator with hysteresis



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Figure 20. Inverting comparator with hysteresis



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For a non-inverting comparator circuit, neglecting input offset voltage and the effect of input biasing current, the input threshold voltages are:

Equation 4

$$V_{TH+} = \frac{R_I}{R_{FB}} \cdot (V_{REF} - V_{OL}) + V_{REF}$$

$$V_{TH-} = \frac{R_I}{R_{FB}} \cdot (V_{REF} - V_{OH}) + V_{REF}$$

V_{OL} is the saturation voltage in low state and V_{OH} is the saturation voltage in high state at the comparator output. The $V_{TH+} - V_{TH-}$ difference determines the hysteresis voltage (V_{HYST}) while their average determines the middle of hysteresis (V_{TRIP}).

Equation 5

$$V_{HYST} = V_{TH+} - V_{TH-} = \frac{R_I}{R_{FB}} \cdot (V_{OH} - V_{OL})$$

$$V_{TRIP} = \frac{V_{TH+} + V_{TH-}}{2} = V_{REF} + \frac{R_I}{R_{FB}} \cdot \left(V_{REF} - \frac{V_{OL} + V_{OH}}{2} \right)$$

In [Equation 5](#) the influence of reference voltage on the trigger voltage level can be seen. The trip point voltage V_{TRIP} (middle of hysteresis) is equal to the reference voltage V_{REF} only when the second part of the equation equals zero, it means when V_{REF} is set just to the

centre of output voltage swing. Otherwise V_{REF} and V_{TRIP} are different and the hysteresis is not centred on V_{REF} .

For calculating R_I , R_{FB} and V_{REF} , two formulas, obtained from [Equation 4](#) and [5](#), can be used:

Equation 6

$$\frac{R_{FB}}{R_I} = \frac{V_{OH} - V_{OL}}{V_{HYST}}$$

$$V_{REF} = \frac{R_I}{2 \cdot (R_I + R_{FB})} \cdot (V_{OH} + V_{OL}) + \frac{R_{FB}}{R_I + R_{FB}} \cdot V_{TRIP}$$

Example of real design of comparator using external hysteresis network:

Task: find resistor values and voltage reference in order to implement 400 mV hysteresis on 1.2 V threshold voltage. Use push-pull comparator TS3021 powered by +5 V source.

Solution: knowing the output voltage level swing and required hysteresis, calculate the resistor ratio and choose the appropriate resistor (in the range of hundreds of k Ω). Then, substituting resistor values and trip point voltage in the second formula, calculate the reference voltage.

For 5 V output swing and hysteresis 400 mV, the ratio of feedback and input resistor is:

Equation 7

$$\frac{R_{FB}}{R_I} = \frac{V_{OH} - V_{OL}}{V_{HYST}} = \frac{5V}{0.4V} = 12.5$$

Appropriate resistors are $R_{FB} = 300 \text{ k}\Omega$ and $R_I = 24 \text{ k}\Omega$. The V_{REF} can now be easily calculated:

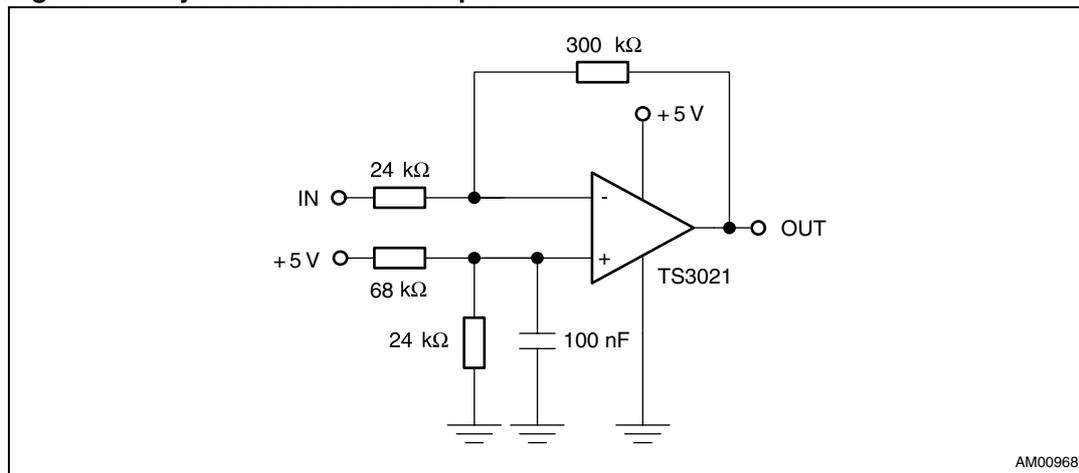
Equation 8

$$V_{REF} = \frac{R_I}{2 \cdot (R_I + R_{FB})} \cdot (V_{OH} + V_{OL}) + \frac{R_{FB}}{R_I + R_{FB}} \cdot V_{TRIP} =$$

$$= \frac{2.4 \cdot 10^4}{2 \cdot (2.4 \cdot 10^4 + 3 \cdot 10^5)} \cdot 5 + \frac{3 \cdot 10^5}{2.4 \cdot 10^4 + 3 \cdot 10^5} \cdot 1.2 = 0.185 + 1.111V = 1.296V$$

[Figure 21](#) shows the final circuit. A reference voltage is generated by the voltage divider supplied from the +5 V source of the comparator. With resistors 68 k Ω and 24 k Ω from the E24 series, the V_{REF} is equal to 1.3 V.

Figure 21. Hysteresis circuit example



4.3 Dynamical hysteresis, example of oscillation issue and the solution

Dynamical hysteresis is another way to eliminate parasitic oscillation during the transition period. When the input signal changes slowly around the reference voltage, an output oscillation may occur. A small capacitor C_{FB} applied between the output and the non-inverting pin boosts up the input signal to go over (or below) the reference voltage faster and in consequence to help reduce oscillations.

The circuit example in [Figure 22](#) shows the usage of the C_{FB} . To induce some output oscillations (on purpose only), consider the case of the application shown in [Figure 22](#): the impedance of the 0.9 V reference voltage is too high because of the 6.8 kΩ resistor. First, consider the situation without C_{FB} when V_{IN+} exceeds V_{IN-} and the output toggles to high state. The fast output edge, together with the parasitic PCB capacity $C_{parasitic}$ between the IN- and OUT pin, causes a positive voltage peak to IN-. V_{IN-} now becomes higher than V_{IN+} . Consequently, the output is returning to low state. The negative peak now goes back to IN-, V_{IN-} is lower than V_{IN+} and the output returns to high. This leads to repetitive oscillations, as shown in [Figure 23](#). The frequency of the oscillations is related to the T_{PD} of the comparator, here it is ~ 10 MHz ($T_{PD} = 50$ ns).

Figure 22. Dynamical hysteresis circuit

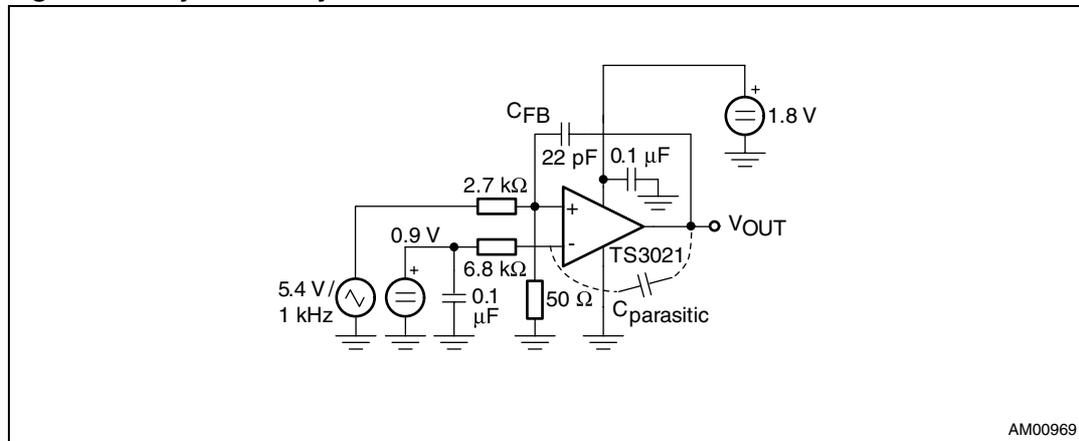
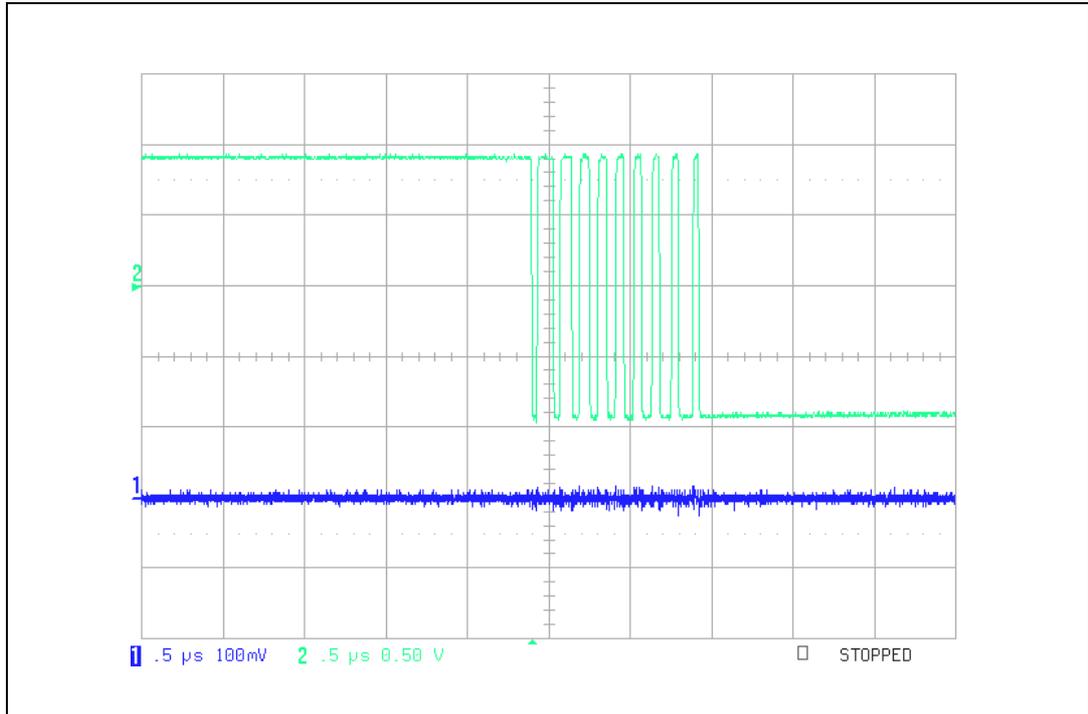


Figure 23. Device oscillation without C_{FB} capacitor (green OUT, blue IN+), time scale 500 ns/div.



Applying a 22 pF feedback capacitor between the IN+ and OUT pin stops the oscillations, as shown in [Figure 24](#) and [Figure 25](#). This feedback capacitor creates a peak (~150 mV for 20 ns) on the IN+ pin which securely eliminates the effects of the peak on V_{IN-} coming from $C_{parasitic}$. The feedback capacitor C_{FB} implements a dynamic hysteresis.

Figure 24. Case with C_{FB} (green OUT, blue IN+), time scale 500 ns/div.

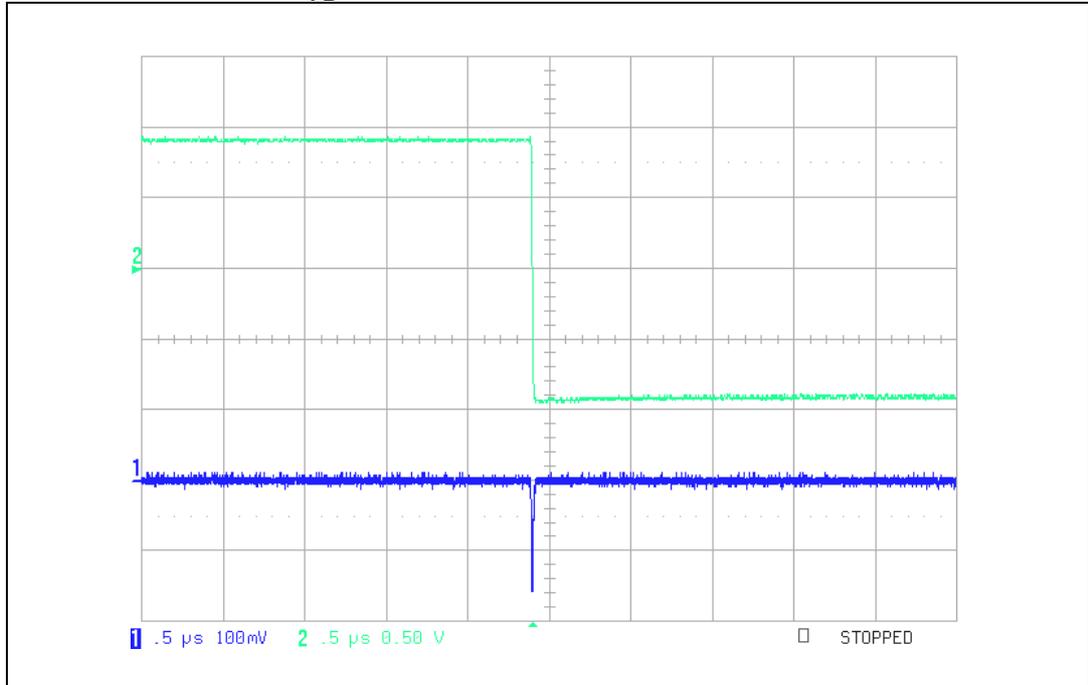
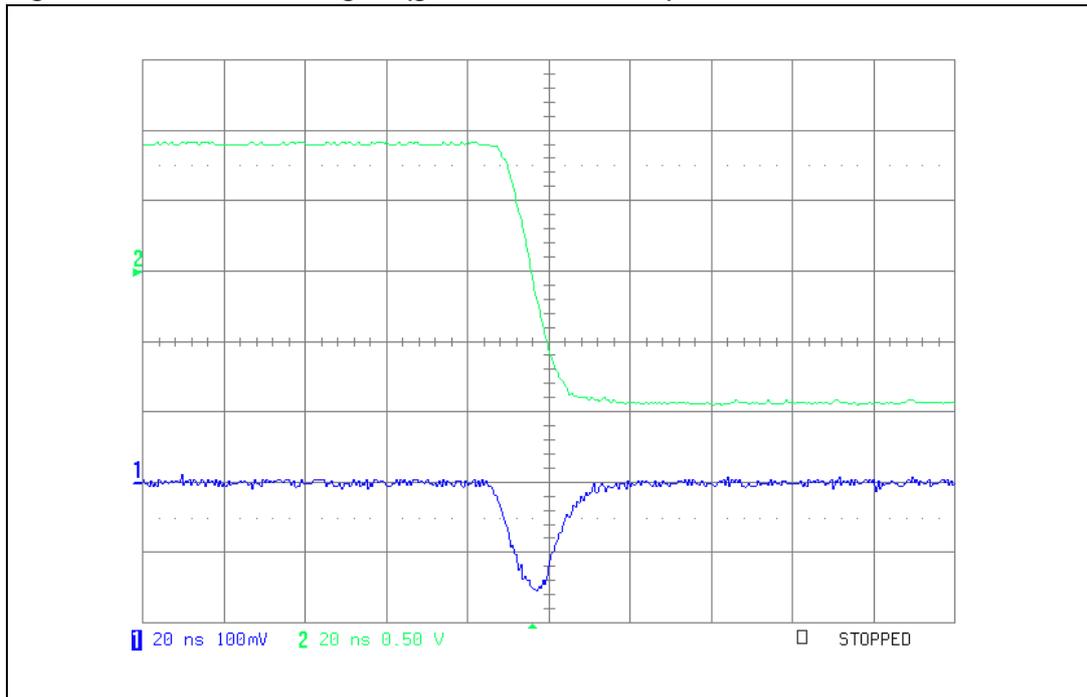


Figure 25. Zoom of the signal (green OUT, blue IN+), time scale 20 ns/div.



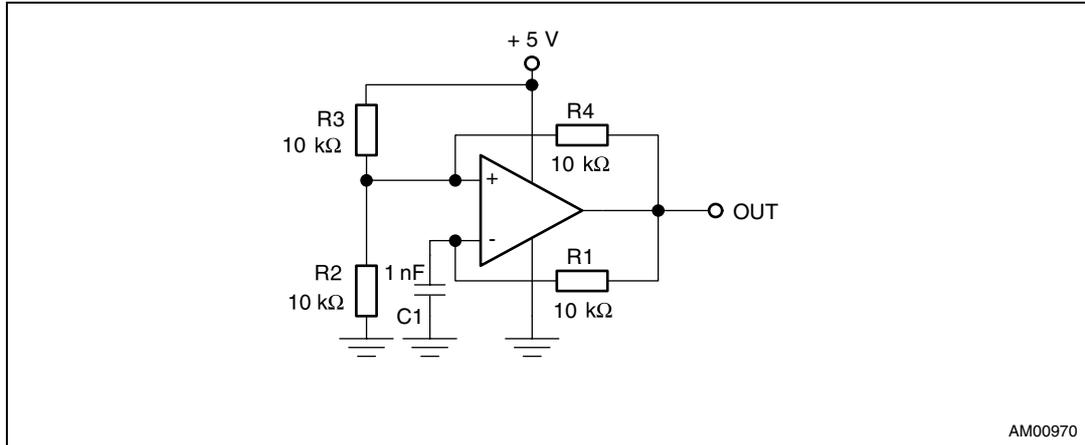
Main general contributors leading to device oscillation

- Parasitic capacity/inductance onboard: long narrow wires, signal and output track close together, device plugged into socket
- Fast (sharp) output edges: faster edge means higher dV/dT and therefore bigger impact of parasitic capacities and inductances on the board
- High impedance on input pins: sensitivity to noise, increased effect of parasitic structures and signal crosstalk
- Poor grounding
- High power supply impedance: inappropriate or missing bypass capacitor
- No hysteresis (static or dynamic) implemented
- Use of high-speed comparator where it isn't necessary.

5 Relaxation oscillator

A relaxation oscillator belongs to the regenerative circuits group. One subgroup is multivibrators which are furthermore classified as monostable, bistable and astable. The relaxation oscillator is an astable multivibrator.

Figure 26. Relaxation oscillator



The circuit in [Figure 26](#) shows a representative circuit of relaxation oscillator based on the TS3021 comparator. It uses both positive and negative feedback. Positive feedback produces voltage hysteresis which has already been described in [Section 4.2](#) Threshold voltages V_{LOW} (from low to high) and V_{HIGH} (from high to low) on the inverting input are given by R_2 , R_3 and R_4 resistors together with output voltage given by power supply voltage.

Considering zero voltage drop at the output see [Equation 9](#):

Equation 9

$$V_{LOW} = V_{CC} \cdot R_2 \parallel R_4 / (R_3 + R_2 \parallel R_4) \text{ and } V_{HIGH} = V_{CC} \cdot R_2 / (R_2 + R_3 \parallel R_4)$$

$$\text{For } R_2 = R_3 = R_4: V_{LOW} = 1/3 \cdot V_{CC} \text{ and } V_{HIGH} = 2/3 \cdot V_{CC}$$

Voltage on the non-inverting input is generated by charging and discharging capacitor C_1 from the comparator output via resistor R_1 in the feedback:

1. While C_1 is charging: $V_{C1(t)} = V_{CC} - (V_{CC} - V_{LOW}) \cdot e^{-t/\tau} = V_{CC} - 2/3 \cdot V_{CC} \cdot e^{-t/\tau}$

Capacitor C_1 is charged at voltage V_{HIGH} after time t_1 :

Equation 10

$$V_{HIGH} = V_{CC} - 2/3 \cdot V_{CC} \cdot e^{-t_1/\tau}$$

$$2/3 \cdot V_{CC} = V_{CC} - 2/3 \cdot V_{CC} \cdot e^{-t_1/\tau}$$

$$-1/3 \cdot V_{CC} = -2/3 \cdot V_{CC} \cdot e^{-t_1/\tau}$$

$$1 = 2 \cdot e^{-t_1/\tau}$$

$$-t_1/\tau = \ln(1/2)$$

$$t_1 = \tau \cdot \ln(2)$$

2. While C_1 is discharging: $V_{C1(t)} = V_{HIGH} \cdot e^{-t/\tau} = 2/3 \cdot V_{CC} \cdot e^{-t/\tau}$

Capacitor C_1 is discharged at voltage V_{LOW} after time t_2 :

Equation 11

$$V_{LOW} = 2/3 \cdot V_{CC} \cdot e^{-t_2/\tau}$$

$$1/3 \cdot V_{CC} = 2/3 \cdot V_{CC} \cdot e^{-t_2/\tau}$$

$$1 = 2 \cdot e^{-t_2/\tau}$$

$$-t_2/\tau = \ln(1/2)$$

$$t_2 = \tau \cdot \ln(2)$$

Because $t_1 = t_2$, the output square signal has 50% duty cycle. The output signal period T is the sum of the time t_1 and the time t_2 :

$$T = t_1 + t_2 = \tau \cdot \ln(4), \text{ where } \tau = R_1 \cdot C_1$$

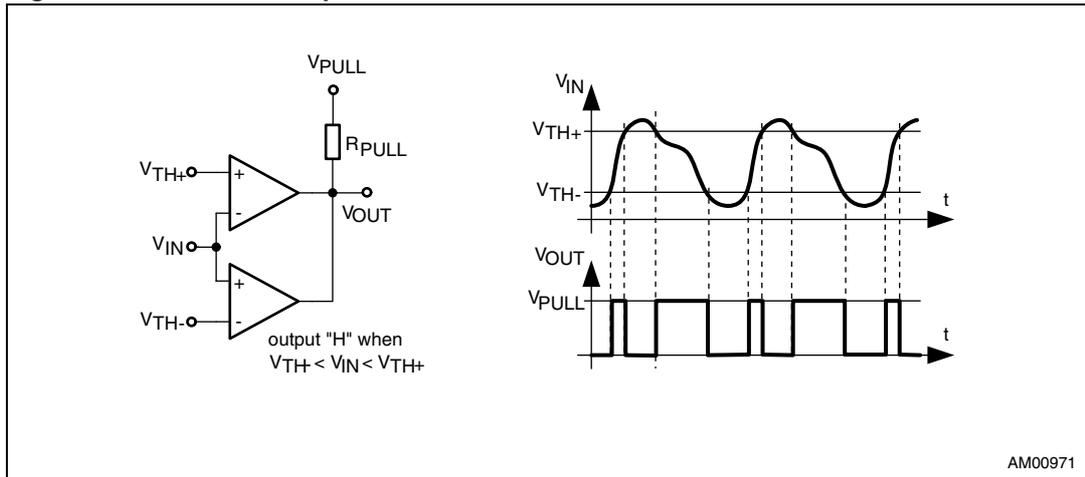
In the configuration described in [Figure 11](#), the output frequency is around 72 kHz.

Output frequency doesn't depend on the power supply voltage. As the TS3021 circuit can work with a wide power supply voltage range from 1.8 V to 5 V, the output signal amplitude has the same value as the power supply due to its rail-to-rail output stage. Frequency can be adjusted simply by changing the value of R_1 or C_1 . In case a different duty cycle is required, R_2 , R_3 and R_4 should not be kept equal.

6 Window comparator

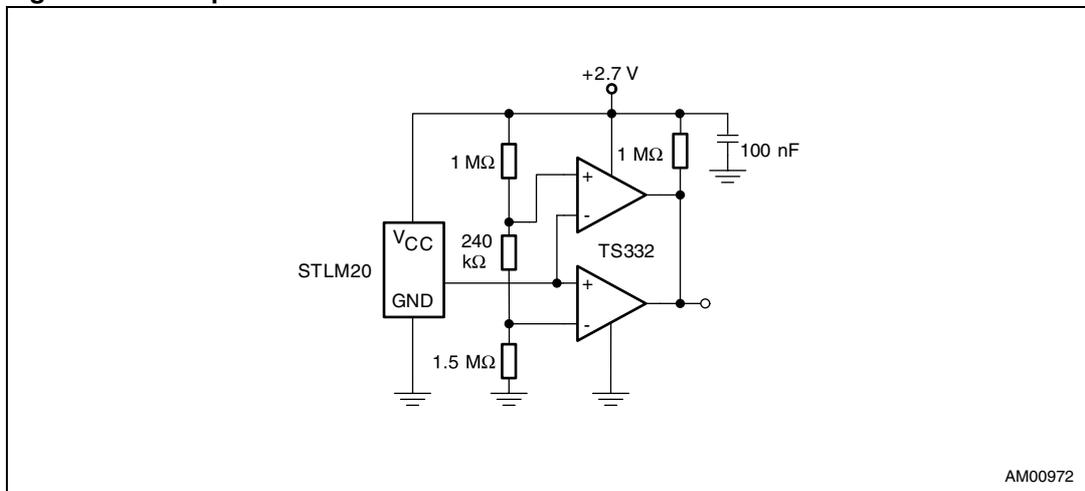
The window comparator is a circuit utilizing two single open drain /collector comparators operating together. It has three inputs. Two of them are dedicated for reference voltage and one for signal input. *Figure 27* illustrates the function of the window comparator. Output is high ($V_{OUT} = V_{PULL}$) when input voltage lies above V_{TH-} and below V_{TH+} , otherwise the output is low (0 V).

Figure 27. Window comparator



AM00971

Figure 28. Temperature control circuit



AM00972

An example of the window comparator application represents a simple temperature controller circuit (*Figure 28*). Based on the TS332 dual comparator and temperature sensor STLM20, the circuit monitors if the temperature holds in the required range ($25 \pm \sim 10 \text{ }^\circ\text{C}$).

The STLM20 is a precision analog output temperature sensor for low current applications. The maximum temperature accuracy of the STLM20 is $\pm 1.5 \text{ }^\circ\text{C}$ (typ. $\pm 0.5 \text{ }^\circ\text{C}$) at ambient temperature of $25 \text{ }^\circ\text{C}$ and V_{CC} of 2.7 V. The STLM20 has a maximum quiescent supply current of $8 \text{ }\mu\text{A}$, therefore self-heating is negligible.

The TS332 is a dual micropower and low-voltage comparator. It can operate with a supply voltage ranging from 1.6 to 5.5 V with only 20 μA current consumption per operator. In addition, rail-to-rail inputs and a temperature range of $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ makes it ideal for a wide range of applications.

With good accuracy about $25\text{ }^{\circ}\text{C}$, the STLM20 transfer function can be described by the parabolic transfer function expressed in [Equation 12](#):

Equation 12

$$V_{\text{OUT}} = (-3.88 \cdot 10^{-6} \cdot T^2) + (-1.15 \cdot 10^{-2} \cdot T) + 1.8639 \text{ [V, } ^{\circ}\text{C]}$$

Based on the STLM20 transfer function equation, for the considered temperature range $25 \pm 10\text{ }^{\circ}\text{C}$, the minimum output voltage $V_{\text{TH-}}$ is obtained at the higher temperature ($35\text{ }^{\circ}\text{C}$) and equals 1.457 V. The maximum output voltage $V_{\text{TH+}}$ is at the lowest temperature ($15\text{ }^{\circ}\text{C}$) and equals 1.691 V.

V_{TH} voltages are generated by a voltage divider. 1 μA current through the divider (I_{DIV}) is a compromise between noise sensitivity and low impact on the supply current of the application. The resistors in the divider are:

$$R_1 \text{ (lower resistor)} = V_{\text{TH-}} / I_{\text{DIV}} = 1.457 \text{ M}\Omega$$

$$R_2 \text{ (middle resistor)} = (V_{\text{TH+}} - V_{\text{TH-}}) / I_{\text{DIV}} = 234 \text{ k}\Omega$$

$$R_3 \text{ (upper resistor)} = (V_{\text{CC}} - V_{\text{TH+}}) / I_{\text{DIV}} = 1.009 \text{ M}\Omega$$

The closest values from the E24 resistor series are: $R_1 = 1.5 \text{ M}\Omega$, $R_2 = 240 \text{ k}\Omega$, $R_3 = 1 \text{ M}\Omega$.

A recalculation of the temperature range can be made with these resistors.

Equation 13

$$I_{\text{DIV}} = V_{\text{CC}} / (R_1 + R_2 + R_3) = 2.7 \text{ V} / (1.5 \text{ M}\Omega + 240 \text{ k}\Omega + 1 \text{ M}\Omega) = 0.985 \mu\text{A}$$

$$V_{\text{TH-}} = I_{\text{DIV}} \cdot R_1 = 1.478 \text{ V}$$

$$V_{\text{TH+}} = I_{\text{DIV}} \cdot (R_1 + R_2) = 1.714 \text{ V}$$

The temperature can be expressed from the voltage of the STLM20:

Equation 14

$$T = -1481.96 + \sqrt{2.1962 \cdot 10^6 + \frac{1.8639 - V_{\text{OUT}}}{3.88 \cdot 10^{-6}}} \text{ (} ^{\circ}\text{C, V)}$$

After substitution we get: $T_{\text{LOW}} = 13\text{ }^{\circ}\text{C}$ and $T_{\text{HIGH}} = 33.2\text{ }^{\circ}\text{C}$.

For better range setting precision, fixed resistors in the voltage divider bridge can be replaced by variable resistors. Note that, temperature setting depends on the supply voltage. Thanks to the micro power TS332 comparator, the power current consumption of the application is typically only 50 μA at $25\text{ }^{\circ}\text{C}$ and max. 74 μA over full temperature range.

7 Revision history

Table 1. Document revision history

Date	Revision	Changes
09-Oct-2012	1	Initial release.

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